Phase Locked Loop Based Frequency Synthesis

Research Summary

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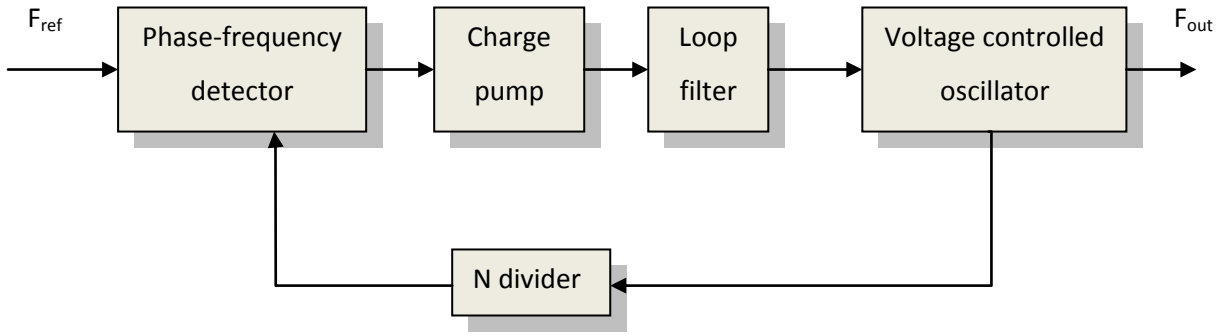
2015

Abstract

A Phase Locked Loop (PLL) is a feedback system combining a voltage controlled oscillator and a phase comparator so connected that the oscillator maintains a constant phase angle relative to a reference signal. The oscillator generates a periodic signal and the phase detector compares the phase of the input signal with the phase of the oscillator's signal, and adjusts the oscillator to keep the phases matched. Keeping the input and output phase in lock means keeping the input and output frequencies the same. PLLs are used in almost every telecommunication electronic devices. In radio transmitters PLL is used to synthesize new frequencies which are multiple of a reference frequency, with the same stability as the reference frequency. They are widely used for synchronization purposes. PLL can be used for recovering a small signal from noisy communication channels and for demodulation of both AM and FM signals. The goal of my project was to do researches about PLL based frequency synthesis.

Frequency synthesizers

Block diagram



A frequency synthesizer consists of a reference signal, phase-frequency detector, charge pump, low pass filter, voltage controlled oscillator, N divider.

The phase detector compares the reference and the output signals and produces an error signal which is proportional to their phase difference. Then the error signal is low pass filtered to ensure the given bandwidth and used to drive the VCO. The output phase of the VCO is fed back through the N divider to the phase-frequency detector, generating a negative feedback

loop. It is very important to have a stable reference frequency. The N divider is usually in the form of a digital counter, so the output frequency can be controlled easily.

Components

1. **Reference signal**

   To achieve high frequency stability mostly quartz crystal oscillators are used. Ideal oscillators would generate a pure sine wave, with a single Dirac impulse in frequency domain. But real oscillators have phase modulated noise components, resulting in noise sidebands.

2. **Phase detector [1]**

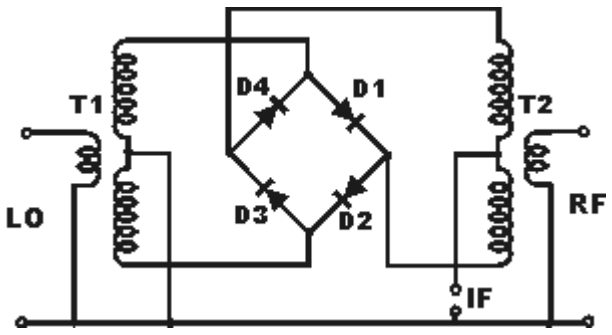
   The phase detector is the core element of a phase locked loop, PLL. Its action enables the phase differences in the loop to be detected and the resultant error voltage to be produced. Two types of phase detectors can be distinguished.

   - **Phase only detectors**

     They simply produce an output that is proportional to the phase difference between the two signals. When the phase difference between the two incoming signals is steady, they produce a constant voltage. When there is a frequency difference between the two signals, they produce a varying voltage. The difference frequency product is the one used to give the phase difference.

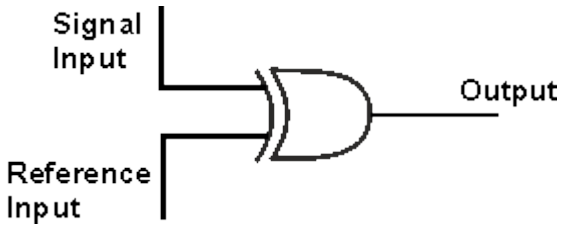
     There are several forms of phase detector that can be used. These fall into the following categories:

     - ***Diode ring mixer phase detector:*** The diode ring phase detector is a simple and effective form of phase detector that can be implemented using a standard diode ring module.



1. Figure Diode ring mixer phase detector

- ***XOR circuit:*** The exclusive OR, XOR phase detector circuit can provide a very useful simple phase detector for some applications.

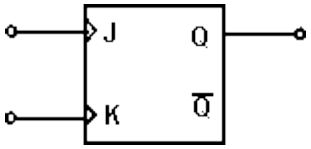


2. Figure XOR circuit

- **Phase - frequency detectors**

  Another form of detector is said to be phase-frequency sensitive. These circuits have the advantage that whilst the phase difference is between ± 180° a voltage proportional to the phase difference is given.

  - ***Edge triggered JK flip flop phase frequency detector:*** This form of phase comparator is used in some designs.

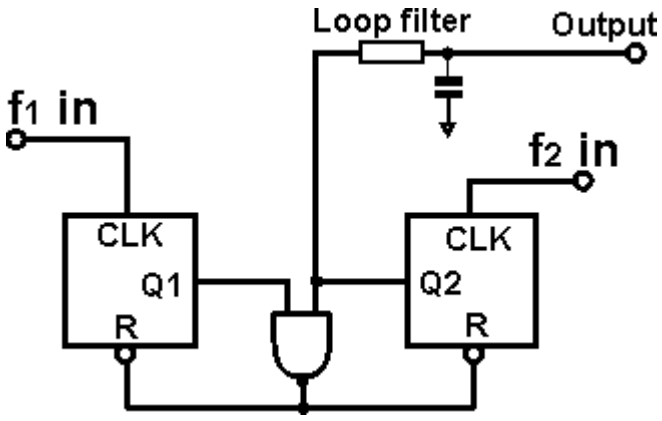


3. Figure JK flipflop

It is a sequentially based circuit and this can be used to provide two signals: one to charge, and one to discharge a capacitor.

- ***Dual D type phase comparator:*** This type of phase comparator is possibly the most widely used form of detector because of its performance and ease of design and use.

  The circuit for the dual D-type comparator uses the two D-type flip flops with the reference and VCO signals being compared entering the clock inputs, one on each D-type. The NAND gate output is fed to the reset, R, inputs of both D-types. The inputs to the NAND gate are taken from the Q outputs and the output to the loop filter being taken from one of the Q outputs.



4. Figure Dual D type phase comparator

Phase detector dead zone

It is found that when the loop is in lock and there is a small phase difference between the two signals, very short pulses are created by the phase detector logic gates. Being very short, these pulses may not propagate and add charge into the charge pump / loop filter. As a result the loop gain is reduced and this forces up the loop jitter / phase noise. To overcome this one solution is to add a delay in the phase detector reset path, i.e. on the output of the NAND gate in the dual D-type detector before the reset terminals of the D-types.

3. Loop filter [2]

This filter is used to filter the output from the phase comparator in the PLL. It is used to remove any components of the signals of which the phase is being compared from the VCO line. It also governs many of the characteristics of the loop and its stability. The loop filter is usually a low pass filter. Loop parameters commonly examined for loop filter design are the loop's gain margin and phase margin.

4. Voltage controlled oscillator [3]

Within a phase locked loop, PLL, or frequency synthesizer, the performance of the voltage controlled oscillator, VCO is of paramount importance. This is because the VCO Voltage Controlled Oscillator performance determines many of the overall performance characteristics of the overall synthesizer.

VCO requirements:

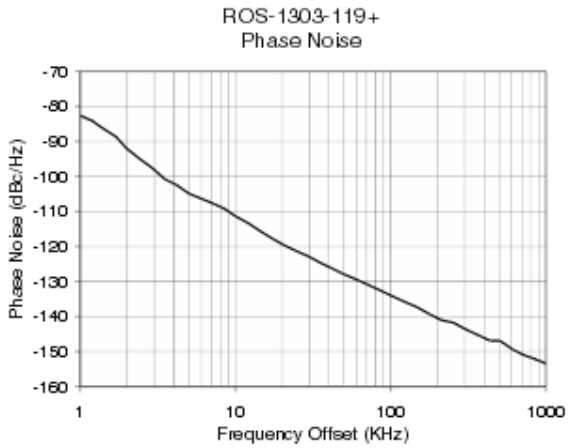
VCO tuning range: It is obvious that the voltage controlled oscillator must be able to tune over the range that the loop is expected to operate over.

VCO tuning gain: The gain of the voltage controlled oscillator is important. It is measured in terms of volts per Hz (or V/MHz, etc). As implied by the units it is the tuning shift for a given change in voltage.

VCO V/f slope: It is a key requirement for any voltage controlled oscillator used in a phase locked loop that the voltage to frequency curve is monotonic, i.e. it always changes in the same sense, typically increasing frequency for increasing voltage. If it changes, as can happen in some instances normally as a result of spurious resonances, etc, this can cause the loop to become unstable.

Phase noise performance: The phase noise performance of the voltage controlled oscillator is of particular importance in some PLL applications - particularly where they are used in frequency synthesizers. Here the phase noise performance of the VCO determines many of the overall phase noise performance characteristics of the overall loop and the overall synthesizer if used in one.

I had the opportunity to use Mini circuits *ROS 1303-119+* surface mount VCO. This VCO can operate in the frequency range of 1011-1270 MHz, with a typical output power level of 7 dBm. Its tuning voltage range is from 0.5V up to 12V. It has a typical tuning sensitivity of 26-39 MHz/V. The following figure shows its phase noise characteristics.



5. Figure VCO Phase noise [4]

5. N divider [5]

Dividers constitute a main function in PLL circuits. A PLL circuit needs to cover a very wide range of continuous divisions for the crystal reference and for the VCO. Two types of dividers are used, high speed and low speed.

- **High Speed Dividers**

For the high-frequency VCO's (200-2500 MHz), dual modulus dividers are employed to achieve a simple continuous division mechanism. For example, to cover 25 MHz with 30 kHz steps requires the generation of about 850 contiguous N values A "P / P+1" dual modulus divider will divide by either P or P+1 based upon external command. It has a Modulus Control (MC) input port (typically TTL or CMOS) controlling the number of times to divide by P or P+1. The lowest contiguous divide ratio for a dual modulus device is given by $P^2 – P$. Specifically, a 16/17 divider allows generation of contiguous divider values above N = 239.

To run high division numbers and allow lower divisions (lower than P^2-P), tri-modulus and even quad-modulus circuits are used. One common configuration is 64/65/72. For a tri-modulus P/(P+1)/(P+R) divider, the minimum continuous divide number, Nmin, is given by: Nmin = (P/R + R + 1) * P + R

For a 64/65/72 divider Nmin = 1096, compared with Nmin = 4032 for a 64/65 divider.

- **Low Speed Dividers**

The second type of divider is the regular programmable counter. These counters typically use CMOS technology, run at frequencies up to 100 MHz, and consume very low power. These counters are used as the reference divider and also as dual modulus control counters. A complete PLL "N" divider is typically implemented using a dual modulus divider controlled by two programmable counters, usually described as the "A counter" which determines the number of times the input is divided by P+1 and the "M counter" which determines the number of times the input is divided by P.

The total division ratio for the divider is given by:

$N = P \cdot A+(P+1) \cdot (M-A)$. Note that when A is incremented by 1, M-A decreases by 1 and the total division ratio, N, increases by 1.

Note also that the minimum required bit size of the A counter is equal to the bit size of P. For 64/65, the A counter has to be of no more than 6 bits (64=26).

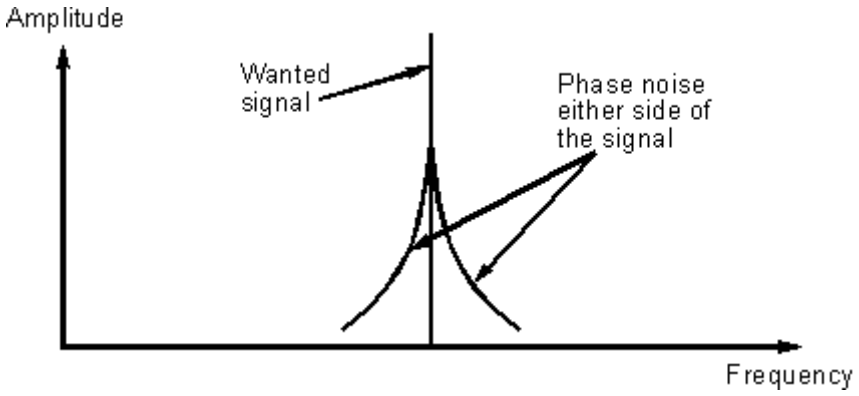
It depends on the type of the N divider that how the synthesizer will work, in Integer-N or in Fractional-N mode.

Phase noise basics [6]

Phase noise or phase jitter is of particular importance, because it reduces the signal quality and hence increases the error rate of the communications link.

A PLL is a type of oscillator, and in any oscillator design, frequency stability is of critical importance.

The term phase noise is used to describe the phase variations that arise as a result of random frequency variations of the signal. The noise arises from general noise in the circuit that manifests itself as frequency variations. The following figure shows the typical phase noise profile of a signal source.

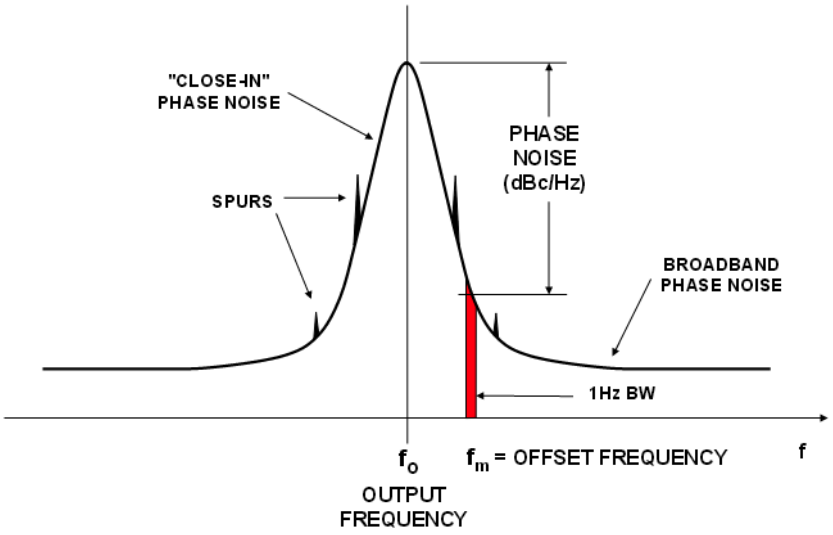


6. Figure Typical phase noise profile of a signal source

Noise in signal sources can be considered in many ways as jitter and variations can occur over different timescales. As a result, stability can be considered in two main forms:

- ***Long term stability*** The long term stability of a signal addresses how the signal varies over a long term, typically hours, days and longer. This addresses subjects such as long term drift etc. It is normally specified in terms of a frequency change in parts per million, etc over a given period of time.
- ***Short term stability*** The short term stability of a signal source focuses on the variations that take place over a much shorter period - typically over periods of less than a second. These variations may be totally random, or they may be periodic. The

periodic variations may be what are termed spurious signals, and the random ones appear as noise.



7. Figure Phase noise profile [7]

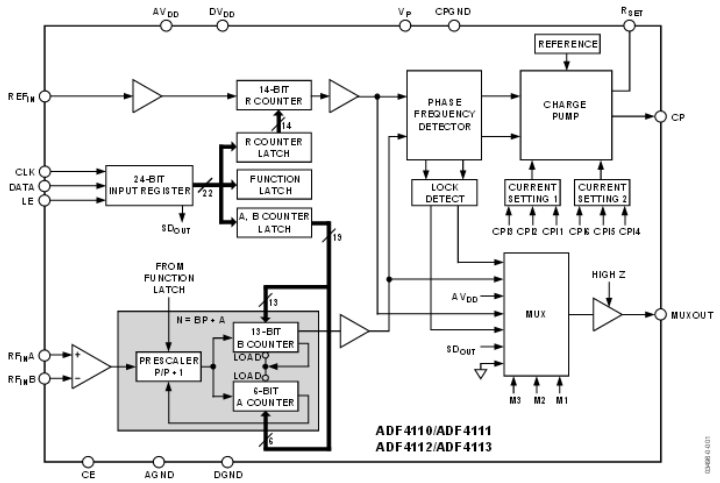
The discrete spurious components could be caused by known clock frequencies in the signal source, power line interference, and mixer products. The broadening caused by random noise fluctuation is due to phase noise. It can be the result of thermal noise, shot noise, and/or flicker noise in active and passive devices.

The phase noise spectrum of an oscillator shows the noise power in a 1 Hz bandwidth as a function of frequency. Phase noise is defined as the ratio of the noise in a 1 Hz bandwidth at a specified frequency offset, fm, to the oscillator signal amplitude at frequency f_o.

Integer-N synthesizer

In the classical Integer-N synthesizer, the resolution of the output frequency is determined by the reference frequency applied to the phase detector. However it is better to use a reference divider (R) between the reference signal and the phase detector. This way only a stable good crystal-based high frequency source is needed, and then it is divided down by the prescaler to the sufficient frequency. The complexity of the N counter has grown over the years. In addition to a straightforward N counter, it has evolved to include a prescaler, which can have a dual modulus. Using a standard prescaler reduces the system resolution to $(F_{REF}/R)\times P$. This issue can be addressed by using a dual-modulus prescaler which has the advantages of a standard prescaler, but without loss of resolution. A dual-modulus prescaler is a counter whose division ratio can be switched from one value to another by an external control signal. [7]

I have managed to get acquainted with Analog Devices ADF4113 Integer-N synthesizer. The ADF4110 family of frequency synthesizers can be used to implement local oscillators in the up conversion and down conversion sections of wireless receivers and transmitters. They consist of a low noise digital PFD (phase frequency detector), a precision charge pump, a programmable reference divider, programmable A and B counters, and a dual-modulus prescaler (P/P + 1). The A (6-bit) and B (13-bit) counters, in conjunction with the dual-modulus prescaler (P/P + 1), implement an N divider (N = BP + A). In addition, the 14-bit reference counter (R counter) allows selectable REFIN frequencies at the PFD input. A complete phase-locked loop (PLL) can be implemented if the synthesizer is used with an external loop filter and voltage controlled oscillator (VCO).



8. Figure ADF4113 block diagram [8]

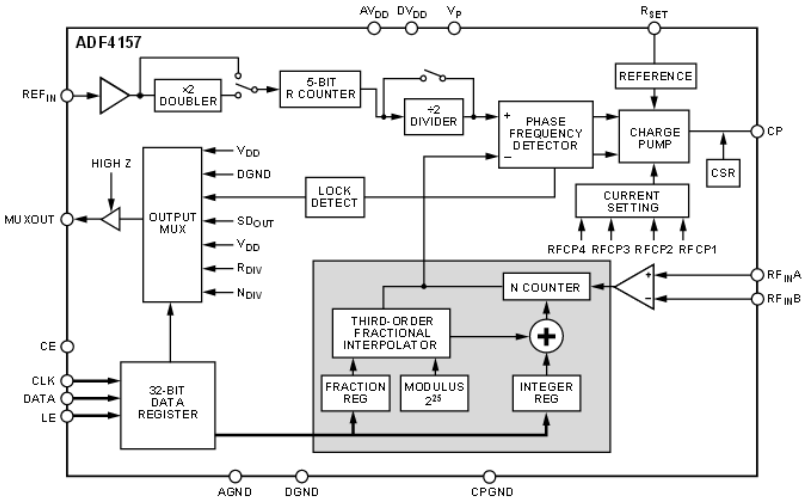
Fractional-N synthesizer

The resolution at the output of an integer-N PLL is limited to steps of the PFD input frequency. Fractional-N allows the resolution at the PLL output to be reduced to small fractions of the PFD frequency, where the PFD input frequency is 1 MHz. It is possible to generate output frequencies with resolutions of 100s of Hz, while maintaining a high PFD frequency. As a result the N-value is significantly less than for integer-N.

Since noise at the charge pump is multiplied up to the output at a rate of 20logN, significant improvements in phase noise are possible. Also offering a significant advantage is the lock-time improvement made possible by fractional-N.

The downside of fractional-N P LLs is higher spurious levels. The fractional-N frequency synthesis is not useful in practical applications unless the fractional spurs are suppressed. Hence, additional circuitry must be added to suppress those fractional spurs. [7]

I have managed to get acquainted with Analog Devices ADF4157 fractional-N synthesizer. The ADF4157 is a 6 GHz fractional-N frequency synthesizer with a 25-bit fixed modulus, allowing subhertz frequency resolution at 6 GHz. It consists of a low noise digital phase-frequency detector (PFD), a precision charge pump, and a programmable reference divider. There is a Σ-Δ based fractional interpolator to allow programmable fractional-N division. The INT and FRAC values define an overall N divider, N = INT + (FRAC/2^{25}). TheADF4157 features cycle slip reduction circuitry, which leads to faster lock times without the need for modifications to the loop filter.



9. Figure ADF4157 block diagram [9]

Spur reduction methods [10]

- **DAC Cancellation Method**

  The phase cancellation method using a digital-to-analog converter (DAC) is a traditional spur reduction method. Since the phase error is compensated in the voltage domain, this method suffers from analog imperfections. The mismatch results mainly from the limited DAC resolution and the limited accuracy of the DAC. This approach is more effective when a sample-and-hold (S/H) phase detector is used instead of the phase/frequency detector (P/FD) since the DAC needs to match only the dc voltage during one reference clock period.

- **Phase Interpolation Method**

  The fact that an N-stage ring oscillator generates N different phases is applied to implement a fractional divider. Since the number of inverters in the ring oscillator is limited, a phase interpolator is used to generate finer phases out of the available phases from the multi-phase ring VCO. By choosing the correct phase among the interpolated phases, a fractional division is achieved. Since the phase edges used for the fractional division ratio are selected periodically, any inaccuracy in the timing interval of the interpolated phase edges generates fixed tones.

- **Random Jittering Method**

  The conventional fractional-N synthesizers suffer from poor fractional spur performance when the analog matching is not well controlled. In addition, design complexity depends on the VCO output frequency. The instantaneous phase error which needs to be cancelled at the phase detector output is the fraction of the VCO output period, which can be as low as 10^{-3} rad. A random jittering approach solves the spur problem in the digital domain by digitally randomizing the digital sequence of the dual-modulus divider control bits.
  At each output of the divider, the random or pseudorandom number generator produces a new random word Pn which is compared with the frequency word K. The frequency word K controls the dual-modulus divider so that the average value can track the desired fractional division ratio. This method suffers from

frequency jitter because the white noise injected in the frequency domain results in $1/f^2$ noise in the phase domain.

- **ΔΣ modulation**

  A ΔΣ fractional-N frequency synthesizer enables direct digital frequency modulation for low cost transmitter design. Basic operation is to use an oversampling ΔΣ modulator to interpolate fractional frequency with a coarse integer divider. While the traditional finite-modulo fractional-N PLLs see more difficulties in spur reduction with higher VCO frequency, the resolution of the ΔΣ fractional-N PLLs does not depend on the VCO frequency. By simply increasing the number of modulation bits, a very fine frequency resolution, e.g. 1 Hz, can be obtained. This method is similar to the random jittering method, but it does not generate a frequency jitter because of the noise shaping property of the ΔΣ modulator. Since the second- or higher-order ΔΣ modulators, in theory, do not generate fixed tones for dc inputs, they effectively shape the phase noise without causing any spur. The operation of the ΔΣ fractional-N PLL is based on following key properties:

  • Frequency interpolation by oversampling;

  • Randomization with high-order modulation;

  • Noise shaping with low frequency noise suppression;

  • Digital input modulation with very fine resolution.

  For fractional-N frequency synthesis, two types of ΔΣ modulators have been used. One is a single-loop delta-sigma modulator (SLDSM), and the other is a cascaded modulator called the MASH modulator.

  Nonlinearity

  The all-digital multi-bit modulator has no linearity problem, but when it is combined with the PLL, the nonlinearity of the phase detector (charge pump) can be a concern. The phase detector converts the digital quantity into an analog quantity by generating the multi-phase errors, and the phase detector nonlinearity is considered a main contributor for nonideal effects of the ΔΣ fractional-N PLL.

  Integer-Boundary Spur

  In theory, the ΔΣ fractional-N PLL with high-order digital modulation can achieve spur-free output spectrum. In practice, sidebands are observed in hardware especially when the VCO frequency is near the integer multiple of

the reference clock frequency, which is often referred to as an integer-boundary spur or a fractional spur. It is shown that the intermodulation between the reference clock path and the feedback clock path generates a beat tone that modulates the VCO and causes the fractional spur.

Quantization Noise

There are several techniques proposed for quantization noise reduction. The phase error cancellation method by using a DAC achieves significant reduction of phase noise and spurs but the performance depends on the high resolution DAC and analog matching, resulting in high design complexity.

- *FIR-Embedded ΔΣ Modulation*

  The semi-digital approach based on a finite-impulse response (FIR) filtering method offers moderate quantization noise reduction without using the DAC. With wide bandwidth, out-of-band noise could be more problematic than in-band noise to meet the phase noise mask required by wireless standards. The hybrid FIR filtering method effectively reduces the out-of-band noise without affecting the PLL loop dynamics. Even though the DAC cancellation method achieves better performance with good analog matching and linearity assumed, the hybrid FIR filtering method provides a straightforward way of noise reduction by simply implementing multiple dividers and phase detectors. The FIR filtering method is especially useful when high order ΔΣ modulators are used.

Summary

Fractional-N PLL represents remarkable progress in PLL technology. Using higher reference frequency allows us to widen loop bandwidth and achieve faster operating times. Fractional-N PLLs can replace multi-loop Integer-N structure, using greater divider ratio. All in all fractional-N PLL offers higher frequency resolution which can be never obtained by Integer-N types. During these past months, I have managed to collect a lot of information about the frequency synthesizer techniques, fractional-N PLLs and do researches about noise reduction techniques.

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