

## Introduction

With the increasing production of electronics devices, the amount of e-waste is also increasing year by year. Electronics industry must find new paths, novel materials or technologies to hold back the harmful disposed waste, generated after the non-functional electronic devices. Regulations were introduced to reduce hazardous substances from electronics (e.g. RoHS, lead-free solder alloys), but due to the increasing waste volumes, new paths should be researched to reduce the harmful nature of the generated waste. Printed Circuit Boards (PCBs) take important part in forming the e-waste, and literature shows little in the applicability of substitute materials for epoxy – such as bio based bioepoxies or different bio based biodegradables. The introduction of novel, environmentally friendly materials is a slow process due to the reduced mechanical and thermal performance of these substrates. Research groups were working on the topic in the last few years – the recent results are summarized in the following part of the paper.

The preceding experiments at the department mainly focused on the comparison of PLA, CA and FR4 substrates as the base material of printed circuit boards. The following limitations were explored: lower melting point and lower glass transition temperature of these materials limit the soldering and manufacturing steps considerably. However, with low melting point solder alloys, several promising applications were achieved, eg. RFID tags with surface mounted ID chips and subtractive PCB track antennas. Also working MP3 players were prepared from biodegradable substrates – where the boards were produced with standard PCB fabrication and SM assembling steps.

Now a new material was put in the focus, namely a glucopyranoside based trifunctional epoxy resin component synthesized with diethylene-toluene-tetramine. The material is more eco-friendly than the usual epoxy in FR4, but not essentially biodegradable.

## Experimental

Our previous works involved PLA and CA materials as PCB substrates. Usually FR4 was also added to the experiments as a reference. Both materials are biodegradable, and have low glass transition temperatures (82 °C and 104 °C respectively); while a common FR4 board uses epoxies with the glass transition temperature of ~140-150 °C. This parameter limited the electronic assembling approaches previously, however with Sn-Bi based solder alloys and careful reflow parameters (low boiling point Galden in a vapour phase soldering oven; local heating with hot gas soldering), the substrates may be used for surface mounted assembly. The average copper peel strength of the produced PCBs was only acceptable when pre-preg was applied between the CA base substrate and the copper layers exceeding the minimum standard value for FR4 boards.

The newly introduced polymer is a bio-based solid glucopyranoside based trifunctional epoxy resin component (GPTE), which is synthesized with diethylene-toluene-tetramine (DETDA) curing agent.

Table 1 summarizes the glass transition temperatures of investigated substrates, which raises the focus on the low T<sub>g</sub> of CA and PLA materials, and also shows the excellent high value T<sub>g</sub> of GPTE, which parameter alone shows a large step up, even from special FR4 materials with higher (170-180 °C) T<sub>g</sub> values suited for special lead-free applications. It is important to see, that while CA and PLA materials are thermoplastic materials, GPTE has thermosetting properties.

**Table 1.** Glass transition temperature of investigated PCB substrates.

Materials	Glass transition temperatures (T <sub>g</sub> )
FR4	~140-150 °C
CA	~104 °C
PLA	~82 °C
GPTE bioepoxy	~210 °C

The GPTE polymer substrate is molded with a Fontune SR100 molder at specific settings, plus optimized pressure forces. Copper foils and pre-preg sheets (standard epoxy+glass fibre material, to enhance top layer

adhesion) are positioned from both sides of the material, to form a package for a two sided base board for subtractive PCB technology. Vias are drilled with standard driller equipment (Posalux Multifor), then the board undergoes wet polishing and drying. Standard photolithography masks are prepared, also electroplating is performed to prepare the trough holes for via copper growth. Before the lamination of the photoresist at 135 °C, there is another round of wet polishing and drying on the boards. The mask pattern is developed with the help of photo resist technology, then copper with 25 µm thickness is developed for the vias. The circuit design is finished on the board with subtractive technology – a tin electroplated layer serves as a mask for the etching. Solder mask can be also applied on GPTE substrates with standard methodology.

The GPTE based boards (along with our previous PLA and CA boards, with reference FR4 boards) were investigated with the following methods. The surface roughness was measured with Alpha-Step 500 type device, which is a stylus type profilometer. The surface hardness was measured with an Innovatest Shore hardness meter with D-mode (30° probe tip angle and 50 N force). The hardness and roughness measurements were performed on 20-20 points on 10 samples. The elasticity measurements were performed on 10-10 samples, in a three point bending tester (Zwick type), after 10 minutes of temperature conditioning. The samples were prepared for 10 mm width, 2 mm thickness and 41,5 mm length dimensions. The moisture absorption measurements were performed with +/- 0,001 g precision laboratory scale. The samples were prepared to have 80x80x2 mm dimensions. Peeling tests were performed with an Instron 5965 type testing system. The tracks for peeling were prepared according to IPC-TM-650. The methodology of the peeling test is described deeper in our previous work. The structural analysis was performed with optical microscopy (Olympus BX-51, with Olympus DP-72 camera), and X-ray microscopy (DAGE XiDAT XD6600).

## Results

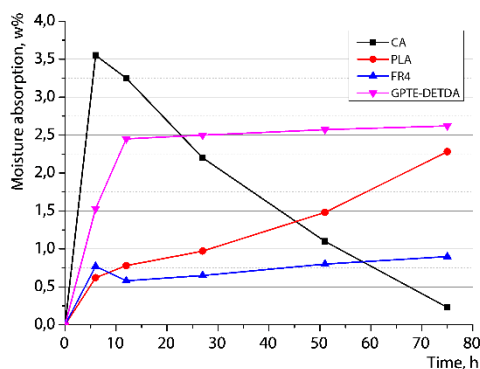
Table 2 shows the measured material parameters of the given bio-based materials, compared to the reference FR4, used in PCB technology.

**Table 2.** Materials parameters

	<b>PLA</b>	<b>CA</b>	<b>GPTE- DETDA</b>	<b>FR4</b>
Average surface roughness, nm	85	89	540-200	650
Surface hardness, Shore D	50	75	86	100
Flexural strength, MPa	46	70	49	476
Elasticity modulus, GPa	1,65	2,65	2,23	245

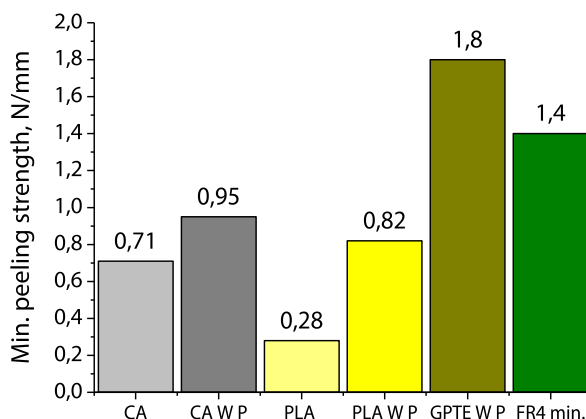
It is important to note, that the polymers or the composite materials do not follow the Hooke's Law directly. The value of elasticity modulus (Young modulus) is given as the initial slope of the load-displacement curve. This value gives little information on practical behavior. The GPTE-DETDA boards give an elastic response for small displacement, then it abruptly cracks for more dynamic load. This limits the overall applicability (or fabrication versatility) of the given material. Table 2 highlights that surface roughness is increased for GPTE-DETDA (compared to PLA and CA) materials, which may result in better copper layer adhesion, from the aspect of PCB wiring. The surface hardness of GPTE-DETDA is better than in the case of the biodegradables, however it does not reach the value of FR4 boards. Flexural strength is similarly low to PLA, an order of magnitude lower than FR4, which also limits sole applicability.

The next figure shows the moisture absorption of the produced boards with the highlighted substrates.



**Fig. 1.** Moisture absorption of PCBs with different substrates

According to the figure the GPTE-DETDA material shows significant absorption characteristic with around three times more moisture absorption, then classical FR4 material; however the nature of the plots are very similar. CA and PLA materials show totally different characteristics. While FR4 and GPTE-DETDA boards slow down with moisture absorption after ~10 hours considerably, CA starts to dry out on ambient air after a dynamic absorption spike; PLA has non-negligible absorption after its initial first the hours as well.



**Fig. 2.** Copper adhesion results – GPTE stands out from the aspect of min. peeling strength values

The next figure show the recorded minimal peeling strength in N/mm unit according to the peel tests performed on different substrates. The W P index means that the copper adhesion was improved with an additional, experimental pre-preg layer between the substrate and the copper. The minimum peel strength value for FR4 substrates, according to the standards, is 1.4 N/mm. This value was achieved only with the GPTE-DETDA material, which means, that (from the aspect of copper adhesion) the substrate performs well.

Mechanical structure analysis with cross section and optical investigation showed an interesting phenomenon which occurs during the layer structure production. The cracking of the bioepoxy can be a critical problem under the solder mask and the pre-preg layer due to its inelastic nature during lamination.

Cracking was also investigated with X-ray microscopy. It affects the mechanical stability of the through hole via as well, showing a critical, and non-acceptable failure in the circuitry – practically crosswise cracks in the copper wall metallizations can also occur. While the electronic performance was not (yet) affected by the cracks during tests, the phenomena must be avoided in the future to enable professional applicability.

## Conclusions

Average surface roughness is a step up from previously investigated PLA and CA materials. Surface hardness is similar (in the same order) for all substrates, however GPTE-DETDA improves upon PLA and CA. Flexural

strength is low and it is important to note, that GPTE-DETDA is very sensitive for dynamic load. This limits fabrication versatility, and overall applicability, due to the resulting cracks in the structure.

It was found, that GPTE-DETDA has significant moisture absorption (considerably higher than FR4). However the copper peel tests showed that copper adhesion is exceptional on the given substrates.

**A fent közölt kutatási eredmények publikálásra kerültek:**

László Gál, Attila Géczy, István Hajdu, Mechanical analysis of experimental sugar-based bioepoxy printed circuit boards, 2017 40th International Spring Seminar on Electronics Technology (ISSE), DOI: 10.1109/ISSE.2017.8000884

Dr. Gál László, Budapest, 2017. 01. 05.